Design of 1.79 µW Operational Amplifier with DC Gain 60 dB

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ABSTRACT

Analog and digital circuits are very important in electronics specially in integrated circuits (ICs). These circuits have changed the face of microelectronics. Being as a key building block, operational amplifier (Op-amp) is useful in vast applications based on analog circuits. Op-amp is the highest power consuming block. Most of the small and portable devices require low power consumption, so the design of low power Op-amp is a challengeable task. A lot of Op-amps have been designed in research work but having trade-off between gain, speed and power as these parameters have contradiction with each other. This work gives design and analysis of a low-power, two stage CMOS based Op-amp with reasonable high gain. The Op-amp is designed in 0.18 µm technology having 1-V supply voltage. The design has been simulated with Cadence software. The total current consumed by the Op-amp is 1.78 µA. The proposed Op-amp consumes low power of 1.79 µW. The amplifier has gain of 60 dB with 67-degree phase margin. The circuit operates at an input frequency of 10 kHz having unity gain frequency of 1.1 MHz. The designed Op-amp has high speed and reasonable output swing with addition to other significant performance parameters.

Due to low power the designed Op-Amp can be used in many implantable and portable devices. The Op-amp can also be used as a front-end building block in circuits like filters, oscillators, comparators, and ADCs to provide the gain or level shifting to the input voltage.

Keywords: Op-amp, CMOS, ICs

1. INTRODUCTION

CMOS based operational amplifiers are the key component used in many analog and mixed signals and systems [1],[4],[9]. Now a days in consumer electronics components, op-amps are required which have better performance parameters such as offset, linearity, stability etc. Speed, power, and accuracy are also very considerable parameters in these systems. The given Op-amp is very useful in analog systems because of its simple architecture, high gain, and low power. Fig.1 gives Op-amp block diagram.

Operational amplifiers (Op-amp) are found to be used in various systems such as smart sensors, active element in preamplifiers, switched-capacitor based filters, data converters, sample and hold circuits [6]. Op-amp of high phase margin high gain, low power and having high bandwidth is useful for biomedical application. In order to have better performance parameters and gain, this paper presents introduction of a CMOS based Op-amp which can be highly useful in low power applications. The given op-amp is two stage to have high gain [5]. The paper is divided such that section 1 describes introduction, section 2 describes Circuit Architecture, section 3 describes parameters table, section 4 gives specifications, section 5 gives simulation results, section 6 gives conclusion and section 7 is about references.

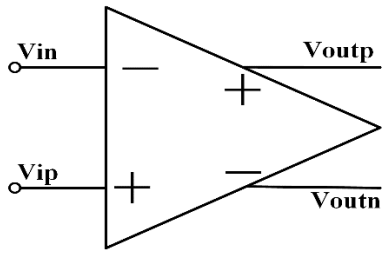

Figure 1: Operational Amplifier

2. Circuit Architecture

Multi-stage op-amp is used a lot in research work by cascading several stages. But one disadvantage of multi-stage is that it may degrades the stability [7]. The proposed Op-amp circuit consist of two stages given in Fig.2. The given circuit is low power as compared to other Op-amp topologies.[2] The single stage comprises of M1-M4 PMOS and M5-M9 NMOS transistors. The circuit is based on inputs differentially based having common source at the second stage. The concept of differential based input is used to give initial gain, whereas second stage is used to increase the gain and optimize the output swing.

For designing a two-stage op-amp having stability, various compensation methods are applied with op-amp. Different compensation methods are used such as capacitor based self-compensation, feed forward compensation having an additional amplifier, negative miller compensation and pole splitting miller compensation. RC miller compensation gives high gain with proper voltage swing as compared to other compensation methods. [3]. The capacitor at the output is connected for phase margin. This compensation capacitor at the output causes to split apart the poles associated with them [8]. Input transistors include NMOS transistors M7 and M8. The first stage output is given as input to second stage.

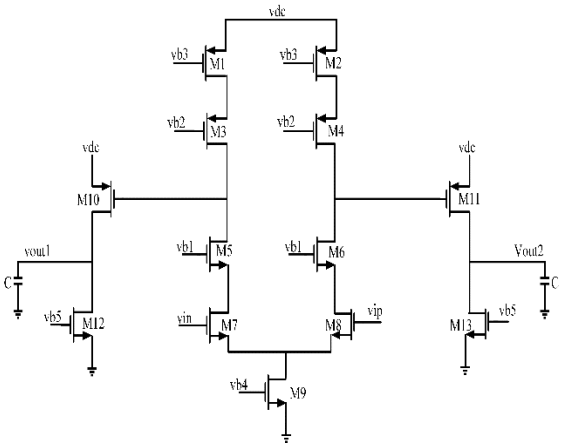

Figure 2: Given Op-amp

3. PARAMETERS TABEL

The proposed Op-amp is designed in cadence software and its different parameters are measured which are given in table.1.

Table 1: Parameters Table

Parameter	Measured Value
DC Gain	60dB
Phase Margin	67°
Unity Gain Frequency	1.1 MHz
Vdd	1-V
Power Dissipation	1.79µW

4. SPECIFICATIONS

The Op-amp is designed by varying width of different transistors so that to acquire the desired gain. The length, width and current across each transistor are given in table.2.

Table 2: Specifications Table

Transistor	W/L	Current
M1, M2	16µm/180nm	555.9nA
M3, M4	6 µm/180nm	555.9nA
M5, M6	9 µm/180nm	555.9nA
M7, M8	220nm/180nm	555.9nA
M9	440nm/180nm	1.11µA
M10, M11	405nm/180nm	338nA
M12, M13	225nm/180nm	338nA

5. SIMULATION RESULTS

The given Op-amp is simulated through cadence software at 180nm CMOS technology. Both transient and AC analysis are carried out with measurement of gain and phase margin. Gain and phase margin of designed Op-amp are given below in Fig.3.

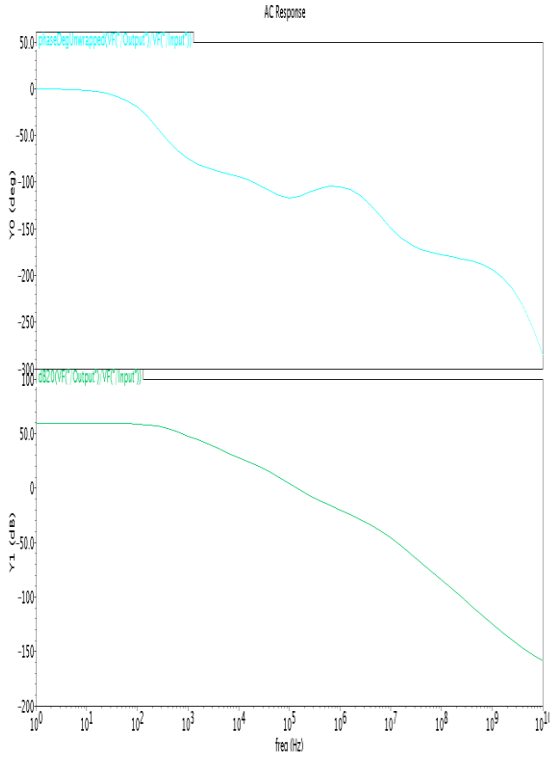

Figure 3: Simulated Result

6. CONCLUSION

Two stage CMOS based Op-amp is designed and simulated through cadence at 0.18µm CMOS technology. The designed Op-amp is low power with reasonable gain. Due to these parameters Op-amp can be used as a front-end building block in many circuits.

7. REFERENCES

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